AMENDMENTS TO THE CLAIMS

Please amend the claims as set forth below:

1. (Cancelled)

2. (Cancelled)

3. (Cancelled).

4. (Cancelled).

5. (Cancelled).

6. (Cancelled).

7. (Cancelled).

8. (Currently Amended) A hysteresis circuit, comprising:

- a sensing amplifier to generate an output signal having an output and two inputs with one of the inputs coupled to an input signal;

- a reference generator coupled to the output and the other one of the inputs of the sensing amplifier and responsive to the output signal to generate an output reference voltage;

- the reference generator including a first originator circuit to generate a first reference voltage on a first reference voltage node; a second originator circuit to generate a second reference voltage on a second reference voltage node; a selector circuit coupled to the first and second originator circuits to provide as the output reference voltage either the first or second reference voltages based upon the output signal undertaking a falling signal transition or a rising signal transition respectively; a voltage supply; and a ground;

- the first originator circuit including ~~a first one of a plurality of p-channel devices or n-channel devices~~ a first p-channel device and a second p-channel coupled in parallel between the voltage supply and the first reference voltage node; and

- the second originator circuit including ~~the non-first one of the plurality of p-channel devices or n-channel devices~~ a first n-channel device and a second n-channel device coupled in parallel between the second reference voltage node and the ground.

9. (Currently Amended) The hysteresis circuit of claim 8, wherein the first originator circuit further includes ~~the plurality of p-channel devices and the second originator circuit includes a plurality of n-channel devices~~ a third p-channel device coupled between the first reference voltage node and the ground.

10. (Currently Amended) The hysteresis circuit of claim [[8]]9, ~~wherein the first originator circuit includes a first, a second, and a third p-channel device and~~ wherein the second originator circuit further includes a ~~first, a second, and~~ a third n-channel device coupled between the second reference voltage node and the voltage supply.

11. (Currently Amended) The hysteresis circuit of claim 10, wherein ~~the reference voltage generator includes a supply voltage and a ground;~~ each of the p-channel and n-channel devices has a source, a drain and a gate; ~~the first originator circuit includes a first reference voltage node having the first reference voltage;~~ the sources of the first and second p-channel devices are coupled to the ~~source~~ voltage supply and the drains of the first and second p-channel devices are coupled to the first reference voltage node; the source of the third p-channel device is coupled to the first reference voltage node and the drain of the third p-channel device is coupled to the ground; the gate of the first p-channel device is coupled to the first reference voltage node; and the gates of the second and third p-channel devices are coupled to the ground.

12. (Currently Amended) The hysteresis circuit of claim 11, wherein ~~the second originator circuit including a second reference voltage node having the second reference voltage;~~ the drains of the first and second n-channel devices are coupled to

the second reference voltage node and the sources of the first and second n-channel devices are coupled to the ground; the drain of the third n-channel device is coupled to the ~~supply~~ voltage supply and the source of the third n-channel device is coupled to the second reference voltage node; the gates of the second and third n-channel devices are coupled to the ~~supply~~ voltage supply; and the gate of the first n-channel device is coupled to the second reference voltage node.

13. (Original) The hysteresis circuit of claim 12, wherein the selector circuit is coupled between the first and second reference voltage nodes.

14. (Currently Amended) The hysteresis circuit of claim 12, wherein the reference voltage generator includes an output reference voltage node having the output reference voltage; and the selector circuit includes a fourth p-channel device and a fourth n-channel device; the fourth p-channel device has the drain coupled to the output ~~voltage~~ reference voltage node and the source coupled to the first reference voltage node and the fourth n-channel device has the drain coupled to the output ~~voltage~~ reference voltage node and the source coupled to the second reference voltage node.

15. (Original) The hysteresis circuit of claim 8, wherein the hysteresis circuit is included in an integrated circuit.

16. (Original) The hysteresis circuit of claim 15, wherein the integrated circuit is a microprocessor.

17. (Currently Amended) A system, comprising:

- an integrated circuit having a reference generator to generate an output reference voltage; a hysteresis circuit responsive to an input signal and the output reference voltage to generate an output signal; the reference generator including a first originator circuit to generate a first reference voltage on a first reference voltage node; a second originator circuit to generate a second reference voltage on a second reference voltage node; a selector circuit coupled to the first and second originator circuits to

provide as the output reference voltage either the first or second reference voltages based upon the output signal undertaking a falling signal transition or a rising signal transition respectively; a voltage supply; and a ground; the first originator circuit including ~~a first one of a plurality of p-channel devices or n-channel devices~~ a first p-channel device and a second p-channel coupled in parallel between the voltage supply and the first reference voltage node; and the second originator circuit including ~~the non-first one of the plurality of p-channel devices or n-channel devices devices~~ a first n-channel device and a second n-channel device coupled in parallel between the second reference voltage node and the ground;

- a DRAM coupled to the integrated circuit; and
- an input/output interface coupled to the integrated circuit.

18. (Original) The system according to claim 17, the integrated circuit further includes a central processing unit, a main memory coupled to the central processor unit and at least one input/output module coupled to the central processor unit and the main memory.

19. (Currently Amended) The system of claim 17, wherein the first originator circuit further ~~includes the plurality of p-channel devices and the second originator circuit includes a plurality of n-channel devices~~ a third p-channel device coupled between the first reference voltage node and the ground.

20. (Currently Amended) The system of claim [[~~17~~]]19, ~~wherein the first originator circuit includes a first, a second, and a third p-channel device and~~ wherein the second originator circuit further includes ~~a first, a second, and~~ a third n-channel device coupled between the second reference voltage node and the voltage supply.

21. (Currently Amended) The system of claim 20, wherein ~~the reference voltage generator includes a supply voltage and a ground;~~ each of the p-channel devices and n-channel devices has a source, a drain and a gate; ~~the first originator circuit includes a first reference voltage node having the first reference voltage;~~ the sources of the first

and second p-channel devices are coupled to the ~~source~~ voltage supply and the drains of the first and second p-channel devices are coupled to the first reference voltage node; the source of the third p-channel device is coupled to the first reference voltage node and the drain of the third p-channel device is coupled to the ground; the gate of the first p-channel device is coupled to the first reference voltage node; and the gates of the second and third p-channel devices are coupled to the ground.

22. (Currently Amended) The system of claim 21, wherein ~~the second originator circuit including a second reference voltage node having the second reference voltage;~~ the drains of the first and second n-channel devices are coupled to the second reference voltage node and the sources of the first and second n-channel devices are coupled to the ground; the drain of the third n-channel device is coupled to the ~~supply~~ voltage supply and the source of the third n-channel device is coupled to the second reference voltage node; the gates of the second and third n-channel devices are coupled to the ~~supply~~ voltage supply; and the gate of the first n-channel device is coupled to the second reference voltage node.

23. (Currently Amended) The system of claim [[20]]22, wherein the selector circuit is coupled between the first and second reference voltage nodes.

24. (Currently Amended) The system of claim [[20]]22, wherein the reference voltage generator further includes an output reference voltage node having the output reference voltage; and the selector circuit includes a fourth p-channel device and a fourth n-channel device; the fourth p-channel device has the drain coupled to the output ~~voltage~~ reference voltage node and the source coupled to the first reference voltage node and the fourth n-channel device has the drain coupled to the output ~~voltage~~ reference voltage node and the source coupled to the second reference voltage node.

25. (Original) The system of claim 17, wherein the integrated circuit is a microprocessor.

26. (Original) The system of claim 17, wherein the input/output interface comprises a networking interface.

27. (Original) The system of claim 17, wherein the system is a selected one of a set-top box, an entertainment unit and a DVD player.